

## **ABSTRACT OF THE DISCLOSURE**

A logarithmic transformer capable of a reduction in circuit scale. A logarithmic transformation upper bit string generating unit detects a highest order bit of logic "1" out of the bits  $b_{n-1}$ , ...,  $b_0$  of input data B as an active bit. Binary data for indicating the bit position S of the active bit is generated as a logarithmic transformation upper bit string  $D_{UP}$  ( $d_{m-1}$ , ...,  $d_{m-p}$ ). Here, based on the number of bits n of the input data B, the number of bits p of the logarithmic transformation upper bit string  $D_{UP}$  ( $d_{m-1}$ , ...,  $d_{m-p}$ ) is set for the relationship  $n = 2^p$ . A logarithmic transformation lower bit string generating unit determines a bit string of order lower than the bit position S, having a predetermined number q of bits, out of the bits  $b_{n-1}$ , ...,  $b_0$  of the input data B. The resultant bit string makes a logarithmic transformation lower bit string  $D_{LOW}$  ( $d_{m-p-1}$ , ...,  $d_0$ ). Then, logarithmic transformation data D having a total number of  $p + q$  bits is generated with the logarithmic transformation upper bit string  $D_{UP}$  ( $d_{m-1}$ , ...,  $d_{m-p}$ ) as the integral part of a logarithmic transformation value resulting from the logarithmic transformation of the input data B and the logarithmic transformation lower bit string  $D_{LOW}$  ( $d_{m-p-1}$ , ...,  $d_0$ ) as the fractional part of the logarithmic transformation value resulting from the logarithmic transformation of the input data B.